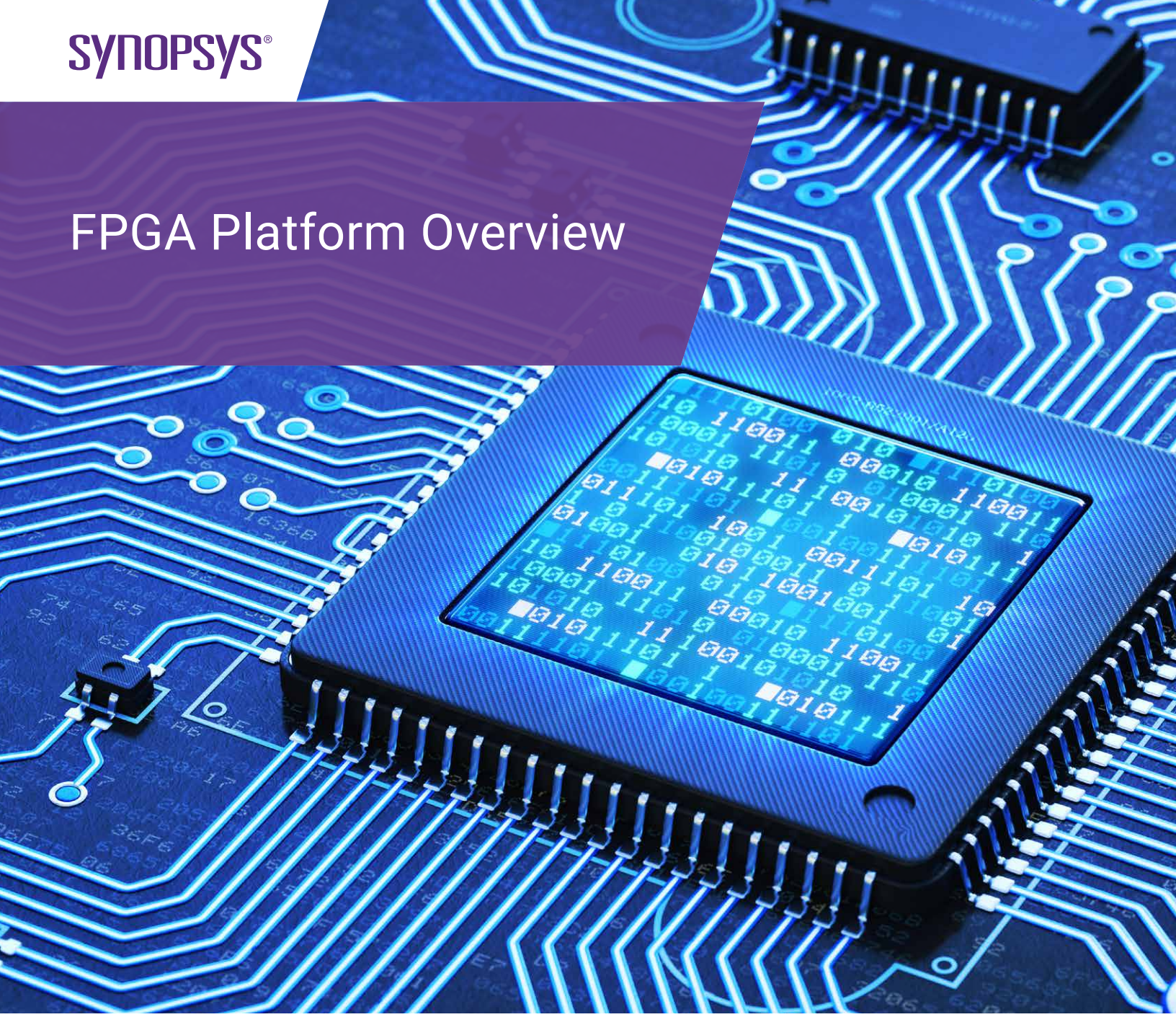
SYNOPSYS®

FPGA Platform Overview



A Comprehensive Solution for FPGA Design

The market is changing for FPGAs. Advancements in lower power, high performance, and low cost are increasing FPGA adoption into applications that have typically been enabled with ASSP/SoCs. FPGA hardware designers face several challenges due to the growing size and complexity of FPGA devices and need the right tools and methodology to complete their designs. Synopsys provides designers an integrated flow from planning through synthesis which helps designers to find and fix bugs earlier and accelerate time-to-first hardware so software development can start on real hardware earlier and the design can be debugged and finalized for market.

FPGA Design Methodology

A typical modern FPGA design is complex with multiple clock and reset domains, memory interfaces, specialized I/O, and integrates third party IP. Better methodologies are needed to help find and fix bugs earlier in the design cycle while providing good results for performance and area to reduce system cost.

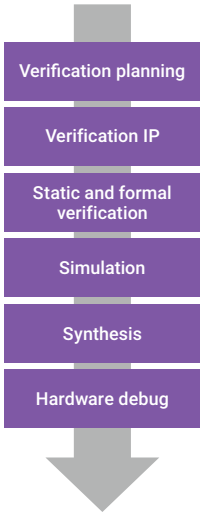


Figure 1: Typical design flow for designing FPGA based applications

An integrated flow helps designers:

- Accelerate time to first hardware
- Easily respond to rapid design changes
- Incrementally apply new modules, find and fix bugs
- Integrate third-party IP easily
- Achieve optimal area and performance quality of results (QoR)
- Accelerate runtimes and deep debug for fast design completion

Verification Planning and Coverage

As the complexity and product requirements increase, designers need a solution for up front verification planning of the FPGA design.

Verdi® Planner (see Figure 2) addresses the growing challenge of verification closure for complex FPGA designs by introducing advanced technology that allows users to quickly create efficient verification plans, integrate third-party and user-defined metrics, link plans to requirement documents, and intuitively track project and test-level metrics across simulation, static checking, formal verification, and Verification IP.

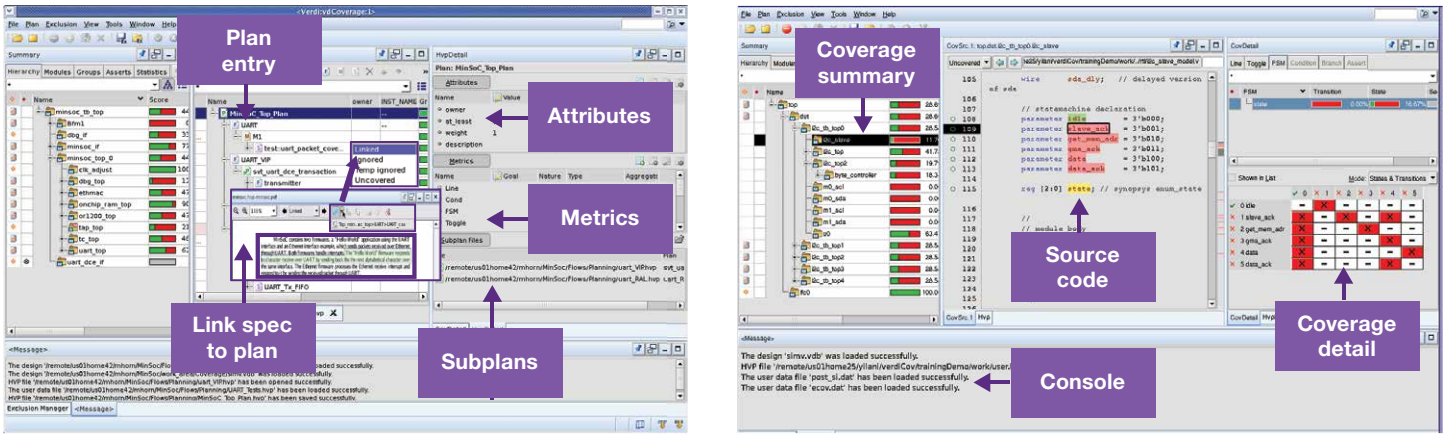


Figure 2: Enabling specification, verification tests and results linking through Verdi

Verifying an FPGA Design with Static, Formal and Simulation

Synopsys provides industry-leading verification solutions, helping designers of broad market applications find and fix bugs faster. With each new generation, designers are adopting a verification strategy that includes simulation, static, and formal verification for both register-transfer level (RTL) and gate level design size and complexity scaling.

Inefficiencies during RTL design usually surface as critical design bugs during the late stages of design implementation. If detected, these bugs will often lead to iterations; if left undetected, they will lead to potential field failures. SpyGlass® linting integrates industry-standard best practices, as well as Synopsys' own extensive experience working with industry-leading customers.

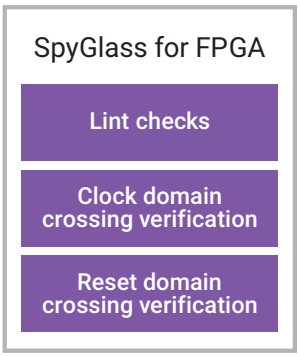


Figure 3: Designers utilize SpyGlass to find and fix bugs earlier in the design

Lint checks include design reuse compliance checks such as STARC and OpenMORE to enforce a consistent style throughout the design, ease the integration of multi-team and multi-vendor IP, and promote design reuse. SpyGlass Lint supports "correct-by-construction" design, leading to early design closure and minimizing costly back-end debugging and iterations.

Among the many verification challenges confronting FPGA designers, clock domain crossings (CDC) are some of the most difficult problems to solve. Today's designs have dozens of asynchronous clock domains, making it difficult to verify using conventional simulation or static timing analysis (STA). Besides the traditional CDC issues, reset domain crossing (RDC) issues can also cause metastability in signals. SpyGlass CDC provides a powerful, comprehensive solution for utilizing library models from different FPGA vendors resulting in more efficient and accurate analysis.

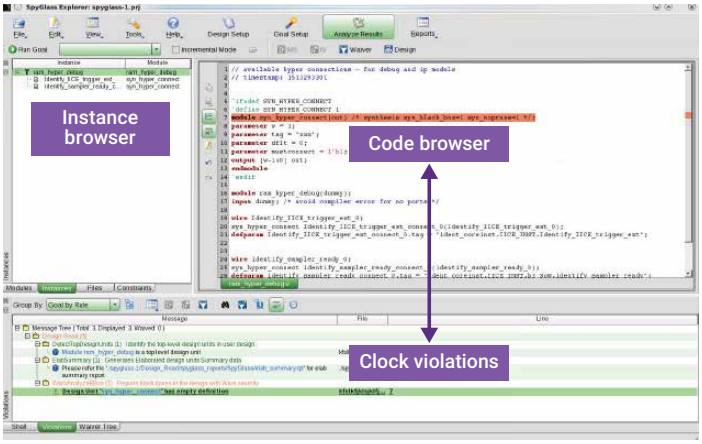


Figure 4: SpyGlass CDC helps designers find clock domain crossing errors

SpyGlass and VC Formal™ combined enable designers and verification engineers to quickly analyze and check RTL designs very early in the design flow, with no need for complex setup, testbenches or stimulus. The VC Formal solution includes a comprehensive set of formal applications that include: Assertion-Based Property Verification, Automatic Extracted Property Checks, Formal Coverage Analysis, Formal Navigator, Sequential Equivalency Checking, Formal Testbench Analyzer with Certitude Integration, Security Verification, Assertion IP, Advanced Debug and Interactivity, Formal Scoreboard, and Formal Coverage.

Once all the static and formal verification is completed, designers will need to simulate their designs. This can pose some unique challenges since both RTL and gate level simulation typically also must be complete. Synopsys provides the industry's highest performance simulation and constraint solver engines with VCS® functional verification solution. The comprehensive VCS solution offers Native Testbench (NTB) support, broad language support and the revolutionary fine-grained parallelism (FGP) simulation technology.

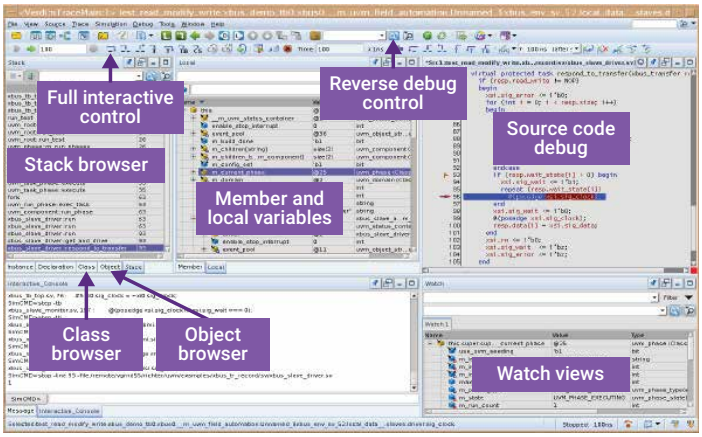


Figure 5 : Fully integrated Verdi with VCS simulation debug

This technology enables far better performance compared to previous technologies by optimally aligning the size and requirements of the simulation tasks and the hardware resources available, allowing far greater effective parallelization and reducing simulation runtime by up to 2X for RTL and 5X for gate-level simulation. In addition, the native integration with Verdi provides verification planning, coverage analysis, and closure.

Synthesis Solutions for Any FPGA Technology

There are many options of FPGA devices, sizes, performance, and integrations available to designers when they need a synthesis solution that addresses a wide range of challenges. The Synplify® synthesis tools provide fast runtime, performance, area optimization for cost and power reduction, multi-FPGA vendor support, support for error detection and mitigation, and incremental and team-design capabilities for faster FPGA design development.

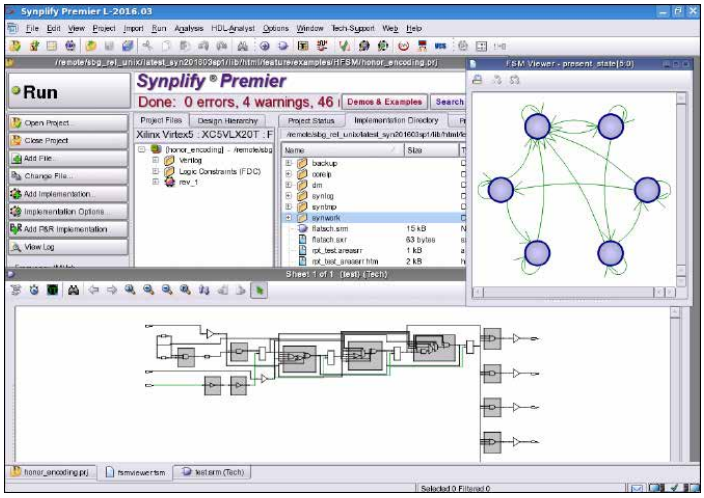


Figure 6: Achieve high performance in small area, more iterations per day and integrated debug with Synplify

Synplify provides designers with several integrations to provide key features for finding and fixing hardware issues early. With the increasing complexity of clock and reset domains requires designers to evaluate the hardware design for errors around clock domain crossing. From within Synplify designers can run SpyGlass CDC directly either in batch or GUI modes. Also, the ability to run VCS from within Synplify allows designers to functionally verify the hardware quickly.

In addition to static and functional verification, the hardware debug environment provides a quick, extensible and easy-to-use method for finding functional errors in FPGA designs that are operating on the board. The wave form viewing and analysis is a direct plug-in to the Verdi environment. This provides a fast path to finding difficult functional errors, editing the RTL to integrate fixes, and simulates the fixes addressing the bug. The overall integrated synthesis environment allows for faster time-to-hardware and ultimately faster time-to-revenue.

Summary

Synopsys is a leading design and verification company with deep experience gained by working with companies to successfully shorten time-to-revenue and minimize schedule risks, which requires extensive upfront verification planning, static and formal verification, simulation and synthesis. FPGA designers can verify the entire design with industry-leading VCS simulation, Verdi debug, SpyGlass static, VC Formal, and silicon-proven Verification IP, as well as gain high performance in small area using Synplify synthesis.

SYNOPSYS®
Silicon to Software™

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